



23rd IEEE NVSMW / 3rd ICMTD '08

May 18th – 22nd 2008,

Club Méditerranée, Opio, FRANCE



Summary of Events

Sunday, 5/18

Registration 4:00PM - 7:00PM
Welcome Cocktail, Dinner 7:30PM - 9:15PM

Monday, 5/19

Breakfast 7:30AM - 8:30AM
Registration 7:30AM - 5:00PM
Session #1 8:30AM - 12:10PM
Lunch 12:30AM - 1:30PM
Committee Luncheon 12:30AM - 1:30PM
Session #2 1:45PM - 5:50PM
Dinner 8:15PM - 9:15PM

Tuesday, 5/20

Breakfast 7:30AM - 8:30AM
Registration 7:30AM - 5:00PM
Session #3 8:30AM - 12:20PM
Lunch 12:30AM - 1:30PM
Session #4 1:30PM - 3:10PM
Panel Discussion 4.00PM- 6:30PM
Dinner 8:15PM - 9:15PM

Wednesday, 5/21

Breakfast 7:30AM - 8:30AM
Registration 7:30AM - 5:00PM
Session #5 8:30AM - 12:20PM
Lunch 12:30PM - 1:30PM
Session #6 1:30PM - 3:10PM
Panel Discussion 4.00PM- 6:30PM
Reception / Gala Dinner 7:30PM - 9:15PM

Thursday, 5/22

Breakfast 7:30AM - 8:30AM
Registration 7:30AM - 9:00AM
Session #7 8:30AM - 12:30PM
Lunch 12:30PM - 1:30PM

23rd Non-Volatile Semiconductor Memory Workshop – 3rd International Conference on Memory Technology and Design

General Chair Richard Eguchi Freescale, USA	Technical Chair Giuseppe Crisenza STMicroelectronics M6, Italy
Finance Chair Pascale Mazoyer STMicroelectronics, France	Local Arrangements Damien Deleruyelle Provence Univ. – IM2NP, France

Technical Committee (Traditional NVM)

Jean-Michel Daga, ATMEL, France
Arthur Wang, Contour Semiconductor, USA
Michael Fliesler, Cypress Semiconductor, USA
Charles Ching-Hsiang Hsu, e-Memory Technology, Taiwan
Erwin Prinz, Freescale, USA
Chung Lam, IBM Research, USA
Jan Van Houdt, IMEC, Belgium
Yanjun Ma, Impinj, USA
Salvatore Lombardo, IMM, Italy
Robert Strenz, Infineon, Germany
Koji Sakui, Intel, USA
Jean Michel Portal, IM2NP, France
Barbara de Salvo, LETI, France
T.C. Lu, Macronix, Taiwan
Ramin Ghodsi, Micron, USA
Bin Yu, NASA, USA
Michiel van Duuren, NXP, Netherland
Giuseppe Iannaccone, Pisa University, Italy
Josef Willer, Qimonda, Germany
Jung-Dal Choi, Samsung, Korea
Klaus Schuegraf, SanDisk, USA
Sung-Yong Chung, Spansion, USA
Jean Michel Mirabel, STMicroelectronics, France
Tamer San, Texas Instruments, USA
Kuniyoshi Yoshikawa, Toshiba, Japan
Yakov Roizin, Tower Semiconductor, Israel
Alan Niebel, WebFeet Research, USA
T.P. Ma, Yale University, USA

Technical Committee (Emerging NVM / RAM)

Lotfi Benammar, ATMEL, France
Tushar Merchant, Freescale, USA
Takayuki Kawahara, Hitachi, Japan
William Gallagher, IBM, USA
Dirk Wouters, IMEC, Belgium
Cyrille Dray, Infineon, Germany
Pierre Fazan, Innovative Silicon Inc., Switzerland
Pranav Kalavade, Intel, USA
Christophe Muller, IM2NP Marseille, France
Pascal Masson, LEAT, France
Atila Alvandpour, Linköping University, Sweden
Karen Attenborough, NXP, Belgium
Doris Keitel-Schulz, Qimonda, Germany
Er-Xuan Ping, Sandisk, USA
David Gilmer, Sematech, USA
Agostino Pirovano, STMicroelectronics M6, Italy
Gregory Wong, WebFeet, USA

GENERAL INFORMATION:

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http://www.icmtd.com/NVSMW-ICMTD08/04-Accommodation_Registration.html

NVSMW Message Center:

Please call the main switchboard and ask for the NVSMW registration table. Messages will be posted regularly on the message center board near the registration table.

Emergencies:

Please go to the nearest phone and dial 9 for help.
For non-emergency issues please request help from Workshop Committee Officers and/or hotel personnel.

Sunday May 18th, 2008

4:00PM – 7:00PM Registration
7:30PM – 8:00PM Welcome Cocktail (Theatre CROISSETTE)
8:15PM – 9:15PM Dinner (ESTEREL Room)

Monday May 19th, 2008

Breakfast 7:30AM – 8:30AM
Registration: 7:30AM - 5PM

Session #1 9:00AM - 12:10PM

Chairs: Richard Eguchi, Freescale, USA
Giuseppe Crisenza, STMicroelectronics M6, Italy
Invited Papers

9:00 AM Opening Remarks: Richard Eguchi
9:10 AM Invited Paper: Ed Doller, Intel, USA, "The evolving role and challenges of non-volatile memory in communication and computing devices"
9:40 AM Invited Paper: Veli Lipponen, Nokia, Finland, "Memories in mobile world evolution"
10:10 AM Break
11:10 AM Invited Paper: B. Eitan / A. Shappir / I. Bloom, Saifun, Israel, "Will charge trapping become the NVM technology of choice?"
11:40 AM Invited Paper: Young Joon Choi, Samsung, Korea, "System requirements and memory subsystem evolution from system perspective"
12:30 PM Lunch Break (ESTEREL Room)
12:30 PM Committee Luncheon (PROVENCE Room)

Monday May 19th, 2008 (continued)

Session #2 1:45 PM-5:50 PM

Chairs: Kuniyoshi Yoshikawa, Toshiba, Japan
Tamer San, Texas Instruments, USA

Floating Gate

- 1:45 PM D.Y. Oh, Samsung, Korea, "Program disturb phenomenon by DIBL in MLC NAND flash device"
- 2:10 PM S.H. Bae, Kyungpook Nat. University, Korea, "Characterization of low frequency noise in floating gate NAND flash memory"
- 2:35 PM D. Wellekens, IMEC, Belgium, "Optimization of Al₂O₃ interpoly dielectric for embedded flash memory applications"
- 3:00 PM S. Shukuri, GENUSION, Japan, "Advantage of floating gate B4-Flash over retention reliability after cycling - characterization by variation of transconductance"
- 3:25 PM Break
- 4:10 PM W.H. Kwon, Samsung, Korea, "3-D channel structure Flash having short channel effect immunity and low Random Telegraph Signal noise"
- 4:35 PM B. Wang, Impinj, USA, "Opportunities and challenges in multi-times-programmable floating-gate logic non-volatile memories"
- 5:00 PM Y.K. Lee, Samsung, Korea, "2T-FN eNVM with 90 nm Logic process for Smart Card"
- 5:25 PM A. Conte, STMicroelectronics, Italy, "A 90 nm embedded page Flash for EEPROM replacement in system on chip"

Floating Gate (Continued)

Tuesday May 20th, 2008

Breakfast 7:30AM – 8:30AM

Registration: 7:30AM - 5PM

Session #3 8:30 AM – 12:20 PM

Chairs: Agostino Pirovano, STMicroelectronics M6, Italy
Dirk Wouters, IMEC, Belgium

Phase Change Memory

- 8:30 AM S.L. Wang, TSMC, Taiwan, "In-Ga-O based double-heater Phase Change memory cell"
- 8:55 AM L. Goux, IMEC, Belgium, "Evidence of the prominent role of the time-under-melt parameter in the reset switching of phase-change line cells"
- 9:20 AM A. Redaelli, STMicroelectronics M6, Italy, "Numerical implementation of low field resistance drift for phase change memory simulations"
- 9:45 AM F. Jedema, NXP-TSMC, Netherland, "Scaling properties of doped Sb₂Te phase change line cells"
- 10:10 AM S.Y. Lee, Korea Inst. of Science and Technology, Korea, "A novel programming method to refresh a long-cycled phase change memory cell"
- 10:35 AM Break
- Phase Change Memory and Emerging Memories**
- 11:05 AM A. Chimenton, Università degli Studi di Ferrara, Italy, "Set of electrical characteristic parameters suitable for reliability analysis of multimegabit phase change memory arrays"
- 11:30 AM P. Zhou, Fudan University, China, "Improvement of endurance and switching stability of forming-free CuxO RRAM"
- 11:55 AM R. Takemura, Hitachi, Japan, "TMR design methodology for spin-transfer torque RAM (SPRAM) with nonvolatile and SRAM compatible operations"
- 12:30 PM Lunch Break (ESTEREL Room)

Session #4 1:30PM-3:10PM

Chair: Salvatore Lombardo, IMM, Italy

Nanocrystal Memory & Emerging Memories

- 1:30 PM S.T. Kang, Freescale, USA, "Si Nanocrystal split gate technology optimization for high performance and reliable embedded microcontroller applications"
- 1:55 PM E. Nowak, CEA/LETI-MINATEC, France, "On the influence of Fin corner rounding in 3D nanocrystal Flash Memories"
- 2:20 PM G. Molas, CEA/LETI-MINATEC, France, "Integration of silicon nanocrystal memory arrays with HfAlOx based interpoly dielectric"
- 2:45 PM J. Buckley, CEA/LETI, France, "On the influence of molecular linker on charge transfer rate in hybrid molecular (Ferrocene)/Silicon field effect memories"
- 3:10 PM Break
- Panel Discussion 4:00 PM - 6:30 PM**
- Chair:** Dirk Wouters, IMEC, Belgium
Joseph Willer, Qimonda, Germany
"New Storage Effects for Non Volatile Memory application"
- 8:15PM – 9:15PM Dinner

Wednesday May 21st, 2008

Breakfast 7:30AM – 8:30AM

Registration: 7:30AM - 5PM

Session #5 8:30 AM – 12:20 AM

Chairs: Jean Michel Mirabel, STMicroelectronics, France
Michiel van Duuren, NXP, Netherland

Embedded Non Volatile Memories

- 8:30 AM N. Akil, NXP/TSMC, Belgium, "Low voltage and fast program and erase SONOS with thick tunnel oxide for low cost embedded EEPROM-like memory applications"
- 8:55 AM N. Ogura, HALO-LSI, USA, "N-Channel complementary pairing in nitride trap memory"
- 9:20 AM T. Ogura, Genusion, Japan, "A highly reliable logic NVM eCFlash (embedded CMOS Flash)" utilizing differential sense-latch cell with charge-trapping storage"
- 9:45 AM M. Fiesler, Cypress Semiconductor, USA, "A 15ns 4Mb NVSRAM in 0.13u SONOS Technology"
- 10:10 AM Break
- Embedded Non Volatile Memories (Continued)**
- 10:40 AM G. Tempel, Infineon Tech., Germany, "Influence and comparison of Cu and Alu metallization schemes on endurance of embedded Flash Memories"
- 11:05 AM Y. Roizin, Tower Semi., Israel, "C-Flash: An ultra-low power single poly logic NVM"
- 11:30 AM J. Power, Infineon Tech., Germany, "Improved retention for a Al₂O₃ IPD embedded Flash cell without top-oxide"
- 11:55 AM G. Fukano, Toshiba, Japan, "A 65nm 1Mb SRAM macro with dynamic voltage scaling in dual power supply scheme for low power SoCs"
- 12:30 PM Lunch Break (ESTEREL Room)

Session #6 1:30PM-3:10PM

Chair: Joseph Willer, Qimonda, Germany

Adv. Dielectrics & Charge Trap. NAND FLASH Memories

- 1:30 PM S.C. Lai, Macronix Int. Taiwan, "An Oxide-Buffered BE-MANOS charge-trapping device and the role of Al₂O₃"
- 1:55 PM S. Sakai, Nat. Institute of Adv. Indust. Science and Tech, Japan
"Highly scalable Fe(Ferroelectric)-NAND Cell with MFIS (Metal-Ferroelectric-Insulator-Semiconductor) structure for Sub-10nm Tera-Bit capacity NAND Flash Memories"

- 2:20 PM C. Jahan, CEA/LETI-MINATEC, France, "Performance enhancement in ultra-scaled SONOS FinFlash by inclusion of high-k dielectric in the gate stack"
- 2:45 PM C.H. Lee, Macronix Int., Taiwan, "Numerical simulation of programming transient behavior in charge trapping storage memory"
- 3:10 PM Break

Panel Discussion 4:00 PM - 6:30 PM

Chair: Eric Gerritsen, IDE@FIX, Bernin - France
"Emerging Solutions"

7:30PM – 8:00PM Cocktail (Theatre CROISETTE)

8:15PM – 9:15PM Gala Dinner

Thursday May 22nd, 2008

Breakfast 7:30AM – 8:30AM

Registration: 7:30AM – 9:00AM

Session #7 8:30 AM – 12:30 PM

Chairs: Koji Sakui, Intel, USA

Jung-Dal Choi, Samsung, Korea

Charge Trapping NAND FLASH Memory

- 8:30 AM T.H. Hsu, Macronix Int., Taiwan, "A study of sub-40nm FinFET BE-SONOS NAND Flash"
- 8:55 AM S.I. Chang, Samsung, Korea, "Reliability characteristics of TANOS (TaN/AIO/SiN/Oxide/Si) NAND Flash memory with Rounded Corner (RC)"
- 9:20 AM H.T. Lue, Macronix Int., Taiwan, "Study of charge trapping vertical location and capture efficiency of SONOS-type devices by gate -sensing and channel -sensing (GSCS) method"
- 9:45 AM M.F. Beug, Qimonda, Germany, "Anomalous erase behavior in charge trapping memory cells"
- 10:10 AM Break
- Charge Trapping NAND FLASH Memory (Continued)**
- 10:40 AM I.C. Yang, Macronix Int., Taiwan, "The impact of interference on multi-level-cell applications in scaled nitride-storage Flash memory"
- 11:05 AM L. Breuil, IMEC, Belgium, "Improvement of TANOS NAND Flash performance by the optimization of a sealing layer"
- 11:30 AM G. Van den Bosch, IMEC, Belgium, "Nitride engineering for improved erase performance and retention of TANOS NAND Flash memory"
- 11:55 AM T. Melde, Qimonda, Germany, "Nitride thickness scaling limitations in TANOS charge trapping devices"
- 12:20 PM Closing Remarks: Richard Eguchi
- 12:30 PM Conference End
- 12:30 PM Lunch (ESTEREL Room)